Multi-standard wideband OFDM RF-PWM transmitter in 40nm CMOS

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***Abstract*— A fully digital 0.9GHz-2.6GHz multimode modulator based on the principle of RF-PWM is presented. It makes use of a delay-line based phase modulator which delays an incoming LO-signal with a resolution of 4ps. The modulator is designed to drive highly efficient switching power amplifiers and support carrier frequencies over a wide range. The modulator has been implemented in 40nm CMOS technology. It achieves an EVM of better than -29dB for a 802.11g 64-QAM OFDM signal. It has also been tested with 40MHz single carrier 64-QAM modulated signals. The measured ACPR is below -30dB up to 2GHz and possible improvements are demonstrated.**

I. INTRODUCTION

Wireless communication networks have witnessed a huge amount of emerging innovation. It is anticipated that the fourth generation mobile systems will be ubiquitous. 4G technology aspires to augment comprehensive and personalized services which exist today. However, to develop a prototype that provides 4G systems' capabilities requires a flexible process especially in an ever-changing specifications and standards world where 5G is also shaping up fast. This provides the scope for development of fully flexible digital transmitters.

Fully digital transmitters based on switched power amplifiers are becoming popular due to their high efficiency and the flexibility provided by the digital hardware. Every generation of process-node provides faster transistors which have enabled digitally-assisted or digital-intensive RF transceivers. They benefit from this technology scaling in terms of power efficiency and die area along with flexibility and speed.

Polar transmitters decompose the baseband signal into amplitude and phase as two separate parts. High efficiency can be achieved as the PA operates as a saturated amplifier in deep compression [1]. However special attention is needed to time-align the phase and magnitude signals. Digital outphasing transmitters decompose the baseband signal into two-constant amplitude phase modulated signals which can be amplified separately by efficient switching PAs whose outputs are summed [2][3]. However an efficient combiner is required to add the PA outputs. In both cases the bandwidth expansion resulting from non-linear transformation makes it challenging to comply with high-speed wireless standards.

In this work, an architecture based on RF pulse-width-modulation (PWM) is explored. Earlier base-band PWM achieves good in-band performance [5]. However it also generates modulated sidebands close to the desired band. To get rid of these close undesired harmonics high Q filters are required which put an additional burden on implementation size, complexity and cost. Therefore an alternative approach to overcome these issues is RF-PWM. In this technique, the harmonics are located at multiples of the carrier frequency (n·fc). With a differential circuit implementation these harmonics can be placed further away from the desired signal band, starting at 3·fc. This helps to significantly reduce the filter requirements compared to a base-band PWM implementation as shown in [10].

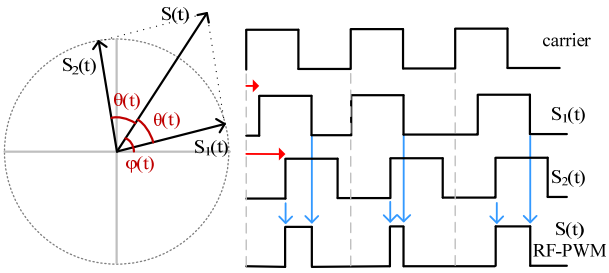

Fig 1: Digital outphasing principle and RF-PWM

The paper is organized as follows. Section II introduces the outphasing concept and the generation of RF-PWM. Section III presents the design and implementation of the proposed transmitter. The measurement results are discussed in Section IV. Finally the conclusions are given in Section V.

II. RF-PWM CONCEPT

A complex modulated signal (eg. 64-QAM) $S(t) = a(t) \cdot \cos(\omega t + \varphi(t))$ generally has amplitude and phase modulation. Due to the amplitude modulation the signal has a variable envelope. As shown in Fig. 1 an outphasing system decomposes the signal $S(t)$ into two constant-amplitude phase modulated components $S_{1,2}(t) = A \cdot \cos(\omega t + \varphi(t) \pm \theta(t))$ whose sum is $S_1(t) + S_2(t) = S(t)$ [4]. The amplitude information a(t) is encoded in the outphasing angle $\theta(t)$ and is given by $\theta(t) = \cos^{-1}(a(t)/2A)$ where A $= \max(a(t)/2)$. As shown in Fig. 1, for digital implementation if two square waves at the carrier f_c, are phase-modulated with phases $\varphi(t) + \theta(t)$ and $\varphi(t) - \theta(t)$ and a logical AND is performed, the resulting signal is a square wave with phase $\varphi(t)$ and duty cycle $d(t) = 0.5 - \theta(t)/\pi$. It can be observed that $d(t)$ is in the range [0 0.5]. From Fourier theory, it can be shown that the fundamental component of this signal is a modulated sinusoid with frequency f_c, phase $\varphi(t)$ and amplitude $A(t) = \sin(\pi\, d(t))$. Hence, RF-PWM is a method where the amplitude information is represented by the pulse width and the phase information is given by the pulse position [8].

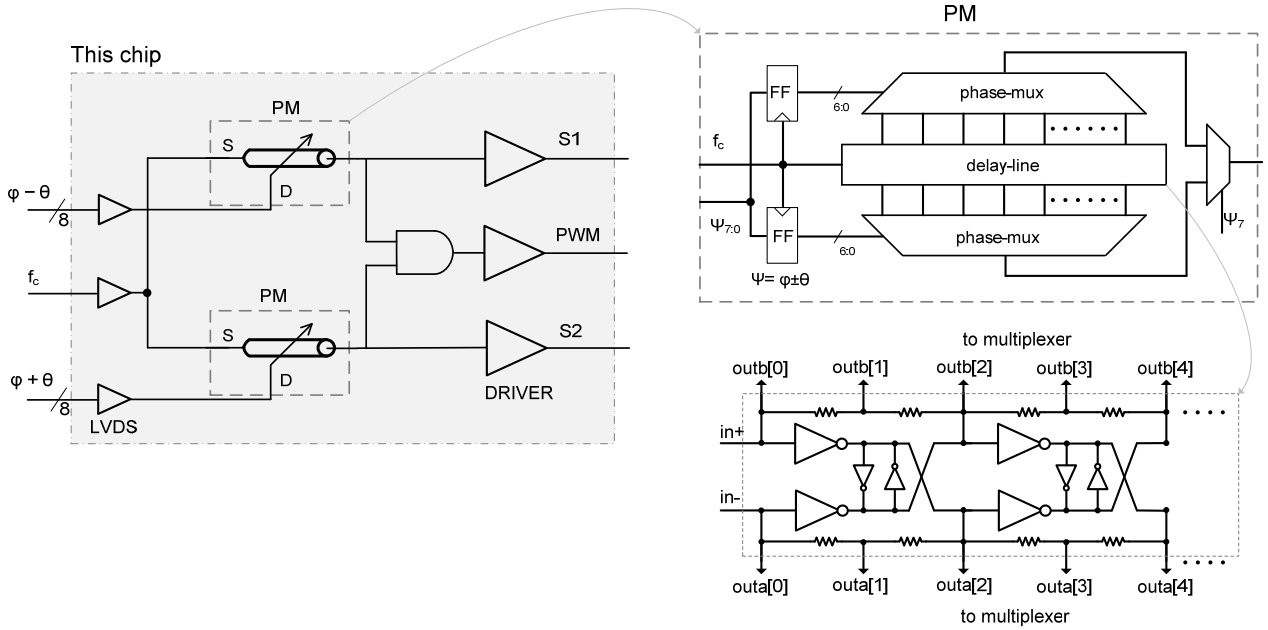

Fig 2 : Single-ended version of the simplified RF-PWM architecture, phase modulator and delay-line implementation.

III. DESIGN AND IMPLEMENTATION

A. Architecture selection

Broadly two RF-PWM transmitter architecture are possible, namely the series and the parallel. In case of the series architecture, the phase modulation $\varphi(t)$ is performed in the first phase modulator (PM) followed by a second PM to perform amplitude modulation [5].The output signal from the first PM again travels through the delay elements of the second modulator (for AM) which can be almost 180°. This can lead to inconsistent output states during that period especially for rapidly varying signals. The delay mismatch impact also adds up along with doubling the complexity of phase-lock. In case of the parallel architecture, one PM is used for each outphasing branch to perform $\psi(t) = \varphi(t) \pm \theta(t)$. As they are updated at the same time, they avoid inconsistent output states. Hence the proposed transmitter is implemented in the parallel architecture as shown in Fig. 2.

B. Design

The input carrier signal along with the input phase-code $\pm\psi_{7:0}$ for the multiplexer are received in a differential manner. A LVDS receiver brings the high-speed digital signals on-chip which modulates the carrier with the corresponding phases. The PWM signal is generated using an AND gate which is placed close to the output bond pad. A driver circuit capable of driving 50Ω is used to get the output signals off-chip. The modulator is designed to drive switching power amplifiers like class-D PAs which are attractive for CMOS implementations.

The select lines for the multiplexer are clocked using the carrier signal itself so as to keep the select lines synchronized with the carrier. The flip-flops are placed very close to the multiplexer inputs. Care was taken to ensure that their delay from the bond-pads to the input of the flip-flop is minimal even at the maximum operating frequency.

The phase modulator (PM) is shown in the top right corner of Fig. 2. It consists of a delay-line along with two phase multiplexers in parallel. As the delay line is implemented in a differential manner, the total delay of the line can handle half of the carrier period which will enable to set phases from 0 to π depending on the least significant bits (LSBs) $\psi_{6:0}$ of the input select codes. Due to the differential nature, phases from π to 2π can be set by interchanging both output signals. This is done by two small multiplexers (not shown in Fig. 2) at the outputs. They are controlled by the most significant bit (MSB) ψ_7 which is clocked with an appropriate delay.

The delay-line consists of multiple unit delay elements as shown in bottom right of Fig. 2. The unit element is based on two forward inverters connected to two small weak inverters whose function is to synchronize the two delay-lines regardless of the delay mismatch. The delay element achieves a unit delay of 8ps and it is improved to 4ps by resistive interpolation [7]. The delay line is composed of 64 delay elements (64·2=128 steps), which are sufficient to support carrier periods up to about 1ns. Few dummy units are added at the end of the line to provide the correct load. Because of the differential implementation this leads to 256 possible values for $\psi(t)$ which corresponds to 8-bit resolution.

The operation at higher frequencies is achieved by using only a part of the delay chain. However by doing so reduces the achievable resolution and increases the quantization noise. Lower frequencies can be supported by reducing the supply voltage of the delay line, which increases the unit delay.

To minimize the impact of mismatch, all the components of the RF path were made larger than the minimal sizing. The delay elements in particular are made large since their mismatch accumulates along the delay lines. Additional precaution is also taken to keep the layout as symmetrical as possible. The critical AND gate is optimized by adding symmetry in the design and layout to handle short pulses generated by the RF-PWM. This can be seen in the AM-AM plot in Fig. 5 which proves the ability to generate low amplitude values.

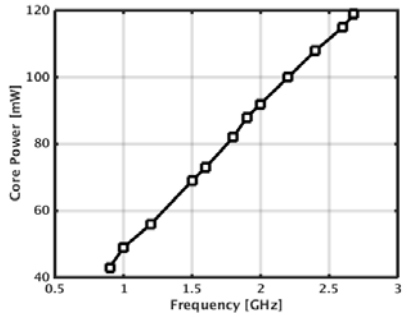

Fig 3 : Power consumption of the core for WLAN 20MHz signal

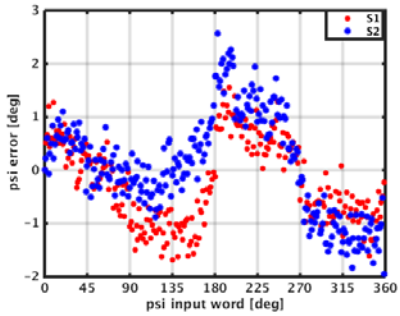

Fig 4: Measured PM-PM at 1GHz

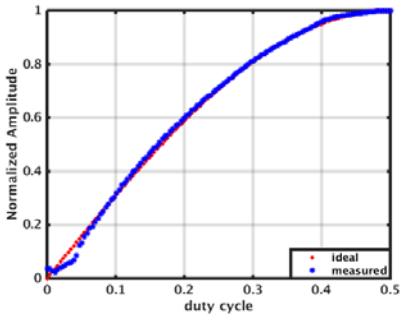

Fig 5: Measured AM-AM at 1GHz

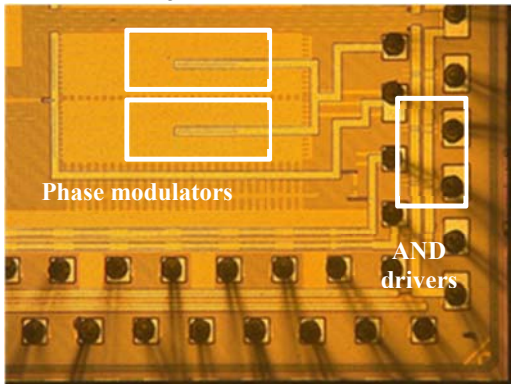

Fig 6 : chip photograph

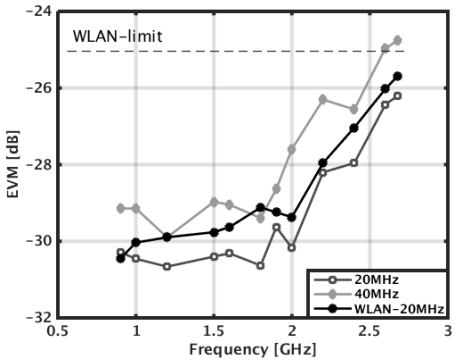

Fig 7: Measured EVM for 64-QAM SC-20MHz, SC-40MHz and WLAN signal at various carrier frequencies.

IV. MEASUREMENTS

The system has been implemented in a 40nm general purpose CMOS process. It operates with a supply voltage of 0.9V. The core area including the phase modulator and input logic converters and output drivers is 0.48 mm^2. The chip photo is shown in Fig. 6.

Fig. 3 shows the power consumption of the core using a 64-QAM WLAN signal. At 1GHz the core consumes 50mW DC-power. It is dominated mainly by the PMs and the multiplexer which operate at carrier frequency and hence scales linearly with frequency. There is an additional overhead of 30mW in the LVDS receivers and 20mW in the drivers. Both of these would be significantly lower when such a system is fully integrated.

A. Static measurements - Locking

Locking of the delay line is crucial for proper operation. The authors in [8] made use of an XOR gate to determine the right supply at which the delay-line is locked. An alternate and more accurate method to perform locking is by down-converting the carrier and measuring its phase. A comparison with respect to the first tap and the N^{th} tap will enable to verify the lock and set the length of the delay-line to N for the given carrier frequency. By setting the right supply voltage, the lock is established.

Using the same setup, the linearity of the modulator can also be measured stand-alone. By sweeping the input phase from 0 to 2π for both the modulators the corresponding output at S1 and S2 terminals are captured by the vector signal analyzer. Fig. 4 shows the measured residual phase error of the PM-PM transfer function at 1GHz. The AM-AM linearity is measured by sweeping the outphasing angle from 0 to $\pi/2$. Thanks to the symmetrical layout of the AND gate, the pulse swallowing is minimized as observed in Fig. 5. The delay-line is locked with 256 elements for this measurement which correspond to 8-bit resolution and the measured error is approximately within 1.4° ($360/2^8$) limit as observed in Fig. 4.

B. Dynamic measurements – Modulated signals

The baseband signals are computed in Matlab and converted to appropriate outphasing signals $\pm\psi_{7:0}$. These signals are transferred to a 16-bit generator which produces the parallel input bits. As the ψ bits are clocked and re-timed using the carrier itself there is no additional requirement for any other reference clock.

Fig. 7 shows measurement results for single-carrier (SC) 20MHz 64-QAM signal achieving an EVM of below -30dB up to 2GHz and reducing to -26dB at 2.6GHz. The SC 40MHz 64-QAM trace also follows a similar trend with about 1.5dB less EVM compared to the 20MHz case. Above 2GHz the effective delay line is below 128 steps and will have resolution less than 7-bits. Due to this the EVM degrades quickly [2]. In both of the SC 64-QAM measurements, the signals were generated with a raised cosine filter with β=0.35 and had a PAPR of 7.3dB. A WLAN 802.11g packet signal with a PAPR of 10.6dB was also measured with the modulator and shows an EVM of better than -29dB from 0.9GHz to 2GHz as observed in Fig. 7. This demonstrates the ability of the modulator to meet the in-band specifications of various standards like EDGE, WCDMA and WLAN.

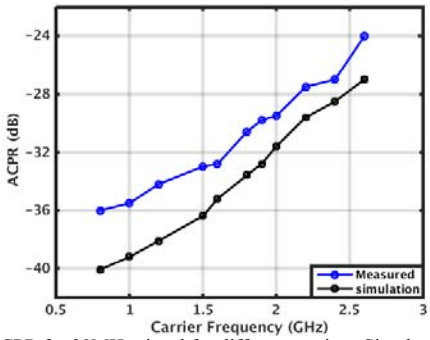

Fig 8: ACPR for 20MHz signal for different carriers. Simulated ACPR using PM-PM and AM-AM characteristics.

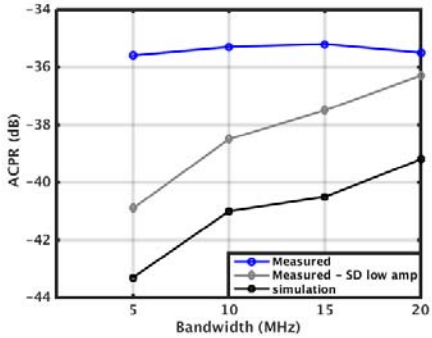

Fig 9: ACPR at 1GHz carrier for different bandwidth DMT signal, Sigma delta for low amplitude level and simulated ACPR

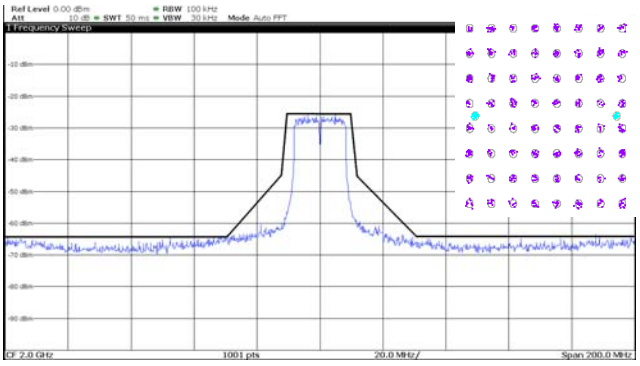

Fig 10 : Transmitted constellation and spectrum of WLAN signal at 2GHz carrier without any correction

The measured ACPR for a 20MHz discrete-multi-tone (DMT) signal with 8dB PAPR for different carrier frequencies is shown in Fig 8. The ACPR is also simulated using the measured PM-PM and AM-AM characteristics. There is a close match between the two as observed in Fig. 8 suggesting that the dynamic effects are minimal. ACPR for different channel bandwidth reaches -35dB at 1GHz as shown in Fig. 9. It can be improved by 5dB when sigma-delta for low amplitude levels is applied. This particular benefit reduces for larger signal bandwidth due to lower over-sampling ratio.

The spectrum along with the transmit mask at 2GHz for a 54Mb/s WLAN 802.11g signal without applying any correction is shown in Fig. 10. The transmitted 64-QAM constellation achieves an EVM of -29.3dB. Table I summarizes the performance and provides a comparison of different techniques used in prior work. The proposed modulator achieves 20MHz operation over a wide range of carrier frequencies and will benefit from scaling as in [2].

TABLE I. COMPARISON SUMMARY OF DIGITAL MODULATORS

	This work	[7]	[8]	[2]	[9]
Technique	**RF-PWM**	RF-PWM	RF-PWM	Out Phasing	RF-DAC
EVM[dB]	**-29**	-29	-38.4	-31.5	-30
BW[MHz] signal	**20 WLAN**	5 WLAN	~5 GMSK	20-40 WLAN	5 WCDMA
Fc[GHz]	**0.9-2.6**	1.0-1.4*	2.2	2.4	1.36-2.51
Tech. [nm]	**40**	40	65	32	65
Resolution	**7-8**	7-8	-	8	13

*carrier up to which WLAN EVM spec is met

V. CONCLUSION

A fully digital transmitter chip was presented based on the principle of RF-PWM. The phase modulator achieves 8-bit resolution and can be locked from 0.9GHz to 2.6GHz. The transmitter's capabilities are demonstrated using a 20MHz 64-QAM WLAN 802.11g signal along with single-carrier 40MHz 64-QAM signal over a wide range of carrier frequencies and achieves EVM better than -29dB. The measured ACPR is below -30dB up to 2GHz. It is improved by 5dB by applying sigma-delta for lower signal bandwidth. Due to the fully digital method, area and performance will benefit from scaling allowing for further improvements.

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